



P280HVN01.0
One Page Spec.

AUO / PID / Travis
2013/08/12

Product Specification



	P280HVN01.0
Resolution	1920x360
Aspect Ratio	16:3
Pixel Size	0.36mm
Brightness	600
Contrast Ratio	3000:1
Display Color	8bit
Frame Rate	60Hz
I/F	2Ch LVDS(51pins) 12V
POL	Haze 2%
Gamma	2.2
CCT	10,000K
Color Gamut	72
Module Chromaticity (X,Y)	(0.280, 0.290)
B/L Power (w)	39W
View Angle	89/89/89/89
BLU	One side edge LED
Outline	725.98(H)*158.9(V)
Thickness	27.6(Front bezel to tcon cover)
Weight	1600g

• Product Feature

- Wide Panel: [16 : 3](#)
- High Brightness: [600 nits](#)
- High Contrast Ratio: [3000:1](#)
- Wide Viewing Angle: [178/178](#)
- With Driver Board

• Schedule

- MP: 9/E

This document is subject to change without notice

LVDS interface



FHD 60 Hz, 8 bit

2Ch LVDS

LVDS 51pin assignment

LCD connector :
JAE FI-RE51S-HF
(JAE)

PIN	Symbol	Description	PIN	Symbol	Description
1	Open	No connection (Internal Open)	26	GND	Ground
2	N.C.	AUO Internal Use Only	27	GND	Ground
3	N.C.	AUO Internal Use Only	28	CH2_0-	LVDS Channel 2, Signal 0-
4	N.C.	AUO Internal Use Only	29	CH2_0+	LVDS Channel 2, Signal 0+
5	N.C.	AUO Internal Use Only	30	CH2_1-	LVDS Channel 2, Signal 1-
6	N.C.	AUO Internal Use Only	31	CH2_1+	LVDS Channel 2, Signal 1+
7	LVDS_SEL	Open/High(3.3V) for NS, Low(GND) for JEIDA	32	CH2_2-	LVDS Channel 2, Signal 2-
8	N.C.	No connection	33	CH2_2+	LVDS Channel 2, Signal 2+
9	N.C.	No connection	34	GND	Ground
10	GND	Ground	35	CH2_CLK-	LVDS Channel 2, Clock -
11	GND	Ground	36	CH2_CLK+	LVDS Channel 2, Clock +
12	CH1_0-	LVDS Channel 1, Signal 0-	37	GND	Ground
13	CH1_0+	LVDS Channel 1, Signal 0+	38	CH2_3-	LVDS Channel 2, Signal 3-
14	CH1_1-	LVDS Channel 1, Signal 1-	39	CH2_3+	LVDS Channel 2, Signal 3+
15	CH1_1+	LVDS Channel 1, Signal 1+	40	N.C.	AUO Internal Use Only
16	CH1_2-	LVDS Channel 1, Signal 2-	41	N.C.	AUO Internal Use Only
17	CH1_2+	LVDS Channel 1, Signal 2+	42	GND	Ground
18	GND	Ground	43	GND	Ground
19	CH1_CLK-	LVDS Channel 1, Clock -	44	GND	Ground
20	CH1_CLK+	LVDS Channel 1, Clock +	45	GND	Ground
21	GND	Ground	46	GND	Ground
22	CH1_3-	LVDS Channel 1, Signal 3-	47	N.C.	No connection
23	CH1_3+	LVDS Channel 1, Signal 3+	48	V _{DD}	Power Supply, +12V DC Regulated
24	N.C.	AUO Internal Use Only	49	V _{DD}	Power Supply, +12V DC Regulated
25	N.C.	AUO Internal Use Only	50	V _{DD}	Power Supply, +12V DC Regulated
			51	V _{DD}	Power Supply, +12V DC Regulated

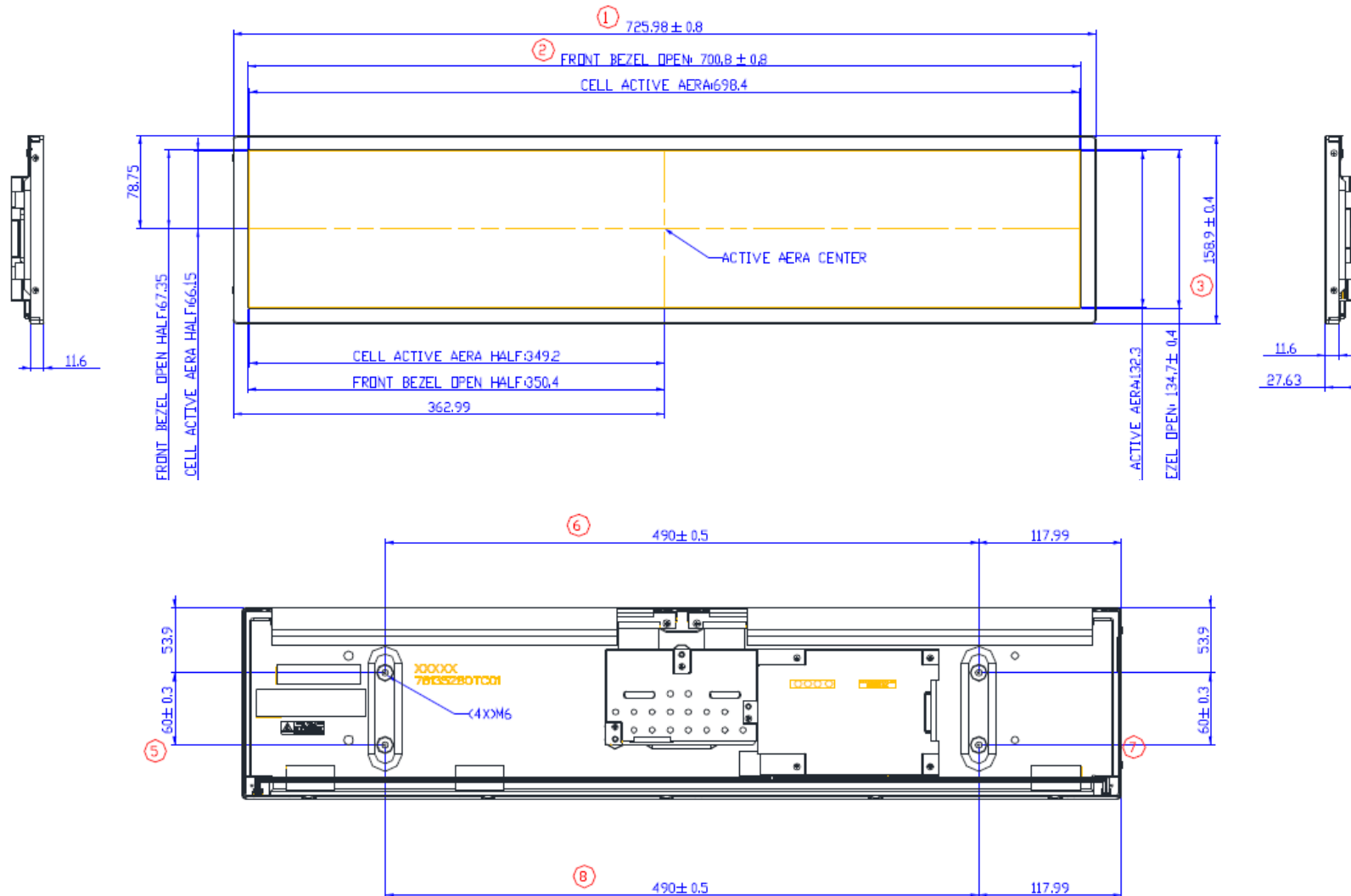
Signal timing (DE only)

Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	T_v	1096	1125	1480	Th
	Active	$T_{disp}(v)$	1080			Th
	Blanking	$T_{blk}(v)$	16	45	400	Th
Horizontal Section	Period	T_h	1030	1100	1325	Tclk
	Active	$T_{disp}(h)$	960			Tclk
	Blanking	$T_{blk}(h)$	70	140	368	Tclk
Clock	Frequency	$F_{clk} = 1/T_{clk}$	50	74.25	82	MHz
Vertical Frequency	Frequency	F_v	47	60	63	Hz
Horizontal Frequency	Frequency	F_h	60	67.5	73	KHz

ME / BLU structure (with D/B)



- BLU structure :LED BLU with D/B
- E-LED Single-side



BLU SPEC.



	Item	Symbol		Condition	Spec			Unit	Note
					Min	Typ	Max		
1	Input Voltage	V _{DDB}		-		24	26.4	VDC	-
2	Input Current	I _{DDB}		V _{DDB} =24V		1.63	1.84	ADC	1
3	Input Power	P _{DDB}		V _{DDB} =24V		39.0	44.1	W	1
4	Inrush Current	I _{RUSH}		V _{DDB} =24V			10	Apeak	2
5	Control signal voltage	V _{Signal}	Hi	V _{DDB} =24V	2	3.3	5.0	VDC	-
			Low		0	-	0.8		3
6	Control signal current	I _{Signal}		V _{DDB} =24V	-	-	1.5	mA	-
7	External PWM Duty ratio (input duty ratio)	D_EPWM		V _{DDB} =24V	5		100	%	4
8	External PWM Frequency	F_EPWM		V _{DDB} =24V	150	160	170	Hz	4
9	DET status signal	DET	HI	V _{DDB} =24V	Open Collector			VDC	5
			Lo		0	-	0.8	VDC	5
10	Input Impedance	Rin		V _{DDB} =24V	300			Kohm	-

Note 1: Dimming ratio= 100%,
(Ta=25±5°C, Turn on for 45minutes)

Note 2: MAX input current at all operating mode, measurement condition Rising time = 20ms (V_{DDB}: 10%~90%)

Note 3: When BLU off (V_{DDB} = 24V , V_{BLON} = 0V) , I_{DDB} (max) = 0.1A

Note 4: Less than 5% dimming control is functional well and no backlight shutdown happened

Note 5: Normal: 0~0.8V ;
Abnormal : Open collector

Driver board pin assignment



LED driver board connector: CI0114MIHR0-LF (Cvilux)

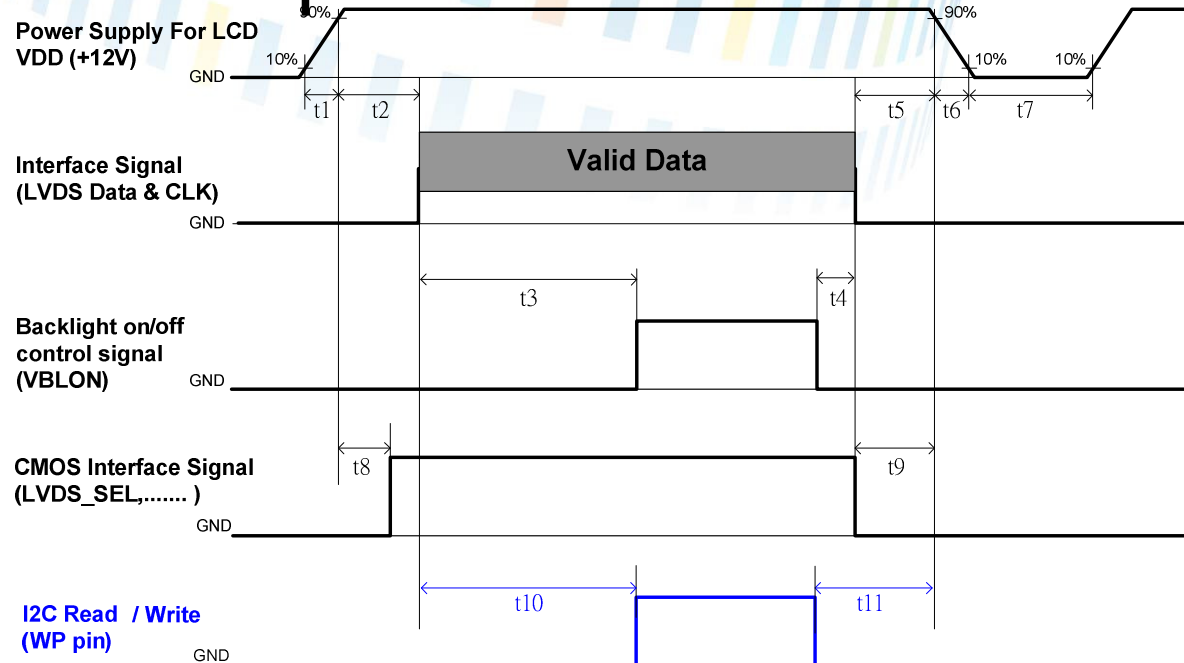
Pin	Symbol	Description
1	VDDDB	Operating Voltage Supply, +24V DC regulated
2	VDDDB	Operating Voltage Supply, +24V DC regulated
3	VDDDB	Operating Voltage Supply, +24V DC regulated
4	VDDDB	Operating Voltage Supply, +24V DC regulated
5	VDDDB	Operating Voltage Supply, +24V DC regulated
6	BLGND	Ground and Current Return
7	BLGND	Ground and Current Return
8	BLGND	Ground and Current Return
9	BLGND	Ground and Current Return
10	BLGND	Ground and Current Return
11	N.C.	No Connection
12	VBLON	BLU On-Off control: BL On : High/Open (2V~5.0V); BL off : Low (0~0.8V/GND)
13	NC	NC
14	PDIM	External PWM (5%~10% Duty)



IF External PWM function less than 5% dimming ratio, Judge condition as below:

- (1) Backlight module must be lighted ON normally.
- (2) All protection function must work normally.
- (3) Uniformity and flicker could not be guaranteed

Power sequence of LCD

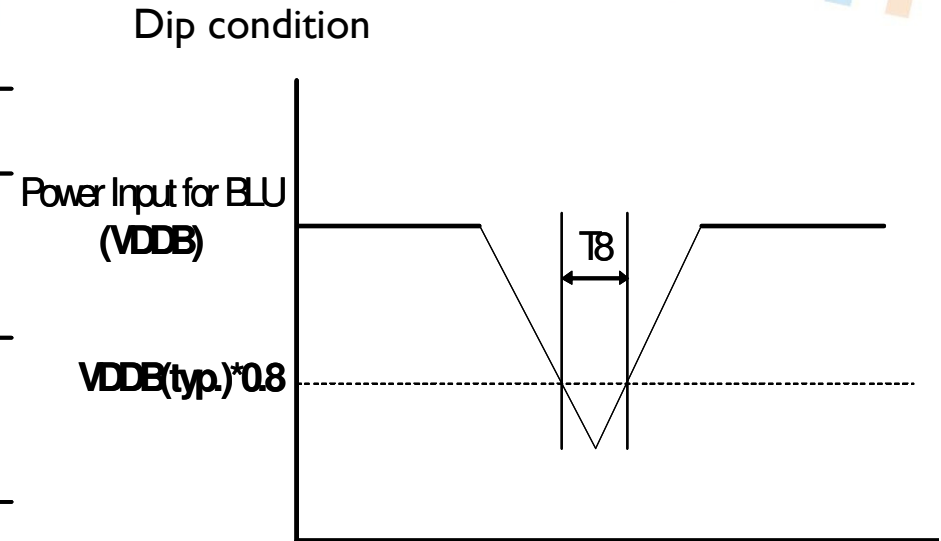
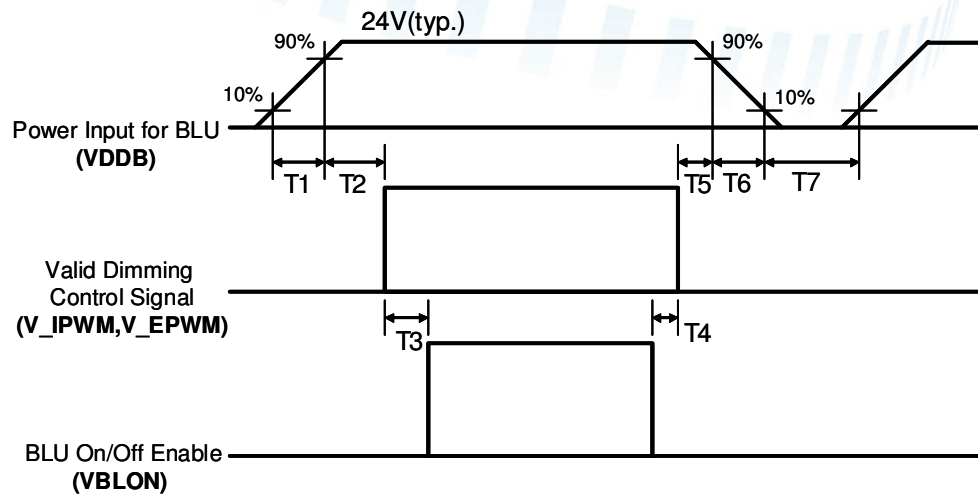


Parameter	Values			Unit
	Min.	Type.	Max.	
t1	0.4	---	30	ms
t2	0.1	---	50	ms
t3	450	---	---	ms
t4	0*1	---	---	ms
t5	0	---	---	ms
t6	---	---	---*2	ms
t7	500	---	---	ms
t8	10*3	---	50	ms
t9	0	---	---	ms
t10	450	---	---	ms
t11	150	---	---	ms

Note:

- (1) t4=0 : concern for residual pattern before BLU turn off.
- (2) t6 : voltage of VDD must decay smoothly after power-off. (customer system decide this value)
- (3) When CMOS Interface signal is N.C. (no connection), opened in Transmitted end, t8 timing spec can be negligible.

Power sequence of Backlight



Parameter	Value			Units
	Min	Typ	Max	
T1	20	-	-	ms *1
T2 (Normal)	500	-	-	ms
T3 (Normal)	250	-	-	ms
T4	0	-	-	ms
T5	1	-	-	ms
T6		-	-	ms
T8	-	-	10	Ms



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